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MATRICES AND GRAPH THEORY IN NETWORKS

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ABSTRACT: Graph theory is a good playground for the exploration of proof techniques in almost all fields of mathematics. Here in this paper let us see its practical application to a switching network. Suppose we are given a box that contain a switching network consisting of some switches and they can be turned on or off from outside, we determine how the switches are connected inside the box, without opening the box, of course with the help of graph theory. Sneak circuit is a latent circuit path or condition that causes undesired function to occur at some certain conditions. Sneak circuit phenomena were found in resonant switched capacitor (RSC) converters. However, because of the complexity of the n-stage RSC converters, the sneak circuit paths are difficult to find out. To solve this problem, graph theory is used to analyze the sneak circuit paths in this paper. Firstly, the n-stage RSC converter was simplified to a directed graph

Key words: Identity matrix, redundant circuit, construction of a graph, switching network

I.INTRODUCTION

INTRODUCTION

Graph theory has a wide range of applications in engineering, electrical network analysis, circuit layout, data structures, operations research, social sciences etc because of its inherent simplicity. It also plays an important role in several areas as switching theory. It begins with very simple geometric ideas and has many powerful applications.

Some Useful Definitions

Definition 1:

Let the number of different circuits in a graph G be q and the number of edges in G be e. Then a circuit matrix B = $[b_{ij}]$ of G is a q by e, (0, 1) – matrix defined as follows:

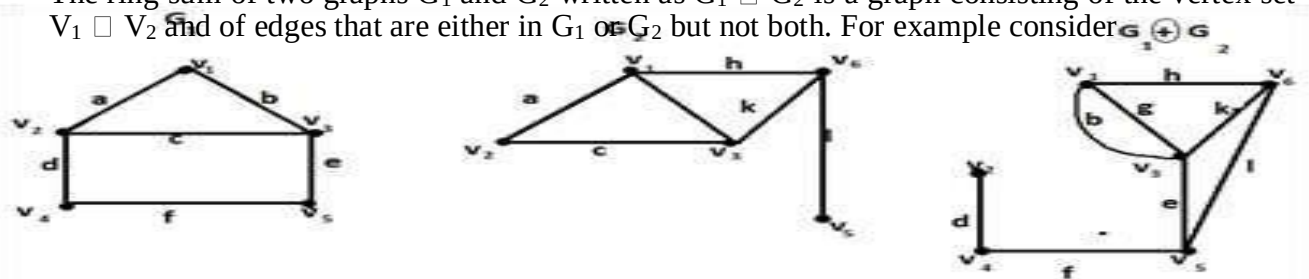
$$b_{ij} = \begin{cases} 1, & \text{if the } i^{th} \text{ circuit includes } j^{th} \text{ edge} \\ 0, & \text{otherwise} \end{cases}$$

Definition 2:

A sub matrix of a circuit matrix in which all rows correspond to a set of fundamental circuits is called a fundamental circuit matrix.

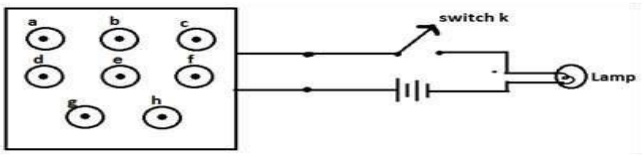
Definition 3:

The ring sum of two graphs G_1 and G_2 written as $G_1 \oplus G_2$ is a graph consisting of the vertex set $V_1 \oplus V_2$ and of edges that are either in G_1 or G_2 but not both. For example consider



Assume that a box contains a switching network consisting of eight switches a,b,c,d,e,f,g and h. The switches can be turned on or off from outside. Let us see how to determine the switching connection inside the box, without opening the box.

First connect a lamp at the available terminals in series with a battery and an additional switch k as shown below:



Let us assume that the following eight combinations light up the lamp.

1. (a,b,f,h,k)
2. (a,b,g,k)
3. (a,e,f,g,k)

Consider the switching network as a graph whose edges represent switches .We can assume that the graph is connected and has no selfloop .Since a lit lamp implies the formation of a circuit; we can regard the preceding list as a partial list of circuits in the corresponding graph. With this list we form a circuit matrix.

B =

	a	b	c	d	e	f	g	h	k
1	1	1	0	0	0	1	0	1	1
2	1	1	0	0	0	0	1	0	1
3	1	0	0	0	1	1	1	0	1
4	1	0	0	0	1	0	0	1	1
5	0	1	1	0	1	0	0	1	1
6	0	0	1	0	0	1	0	1	1
7	0	0	1	0	0	0	1	0	1
8	0	0	0	1	0	0	0	0	1

Next to simplify the matrix, we should remove the obviously redundant circuits. Observe that the following ring sum of circuits give rise to other circuits.

$$(a,b,g,k) \oplus (c,f,h,k) \oplus (c,g,k) = (a,b,f,h,k)$$
$$(a,b,g,k) \oplus (a,e,h,k) \oplus (c,g,k) = (b,c,e,h,k)$$
$$(a,e,h,k) \oplus (c,f,h,k) \oplus (c,g,k) = (a,e,f,g,k)$$

Therefore we can delete the first, third and fifth rows from matrix B, without any loss of information. Remaining is a 5 by 9 matrix B_1.

	a	b	c	d	e	f	g	h	k
	1	1	0	0	0	0	1	0	1
	1	0	0	0	1	0	0	1	1
B_1 =									
	0	0	1	0	0	1	0	1	1
	0	0	1	0	0	0	1	0	1
	0	0	0	1	0	0	0	0	1

Our next goal is to bring matrix B_1 to the form $B_f = [\, I_{fr} / B_r]$. For this we interchange columns to get B_2:

	b	e	f	g	d	a	c	h	k
	1	0	0	1	0	1	0	0	1
	0	1	0	0	0	1	0	1	1
B_2 =									
	0	0	1	0	0	0	1	1	1
	0	0	0	1	0	0	1	0	1
	0	0	0	0	1	0	0	0	1

	b	e	f	g	d	a	c	h	k
	1	0	0	0	0	1	1	0	0
	0	1	0	0	0	1	0	1	1
B_3 =	0	0	1	0	0	0	1	1	1
	0	0	0	1	0	0	1	0	1
	0	0	0	0	1	0	0	0	1

Adding the fourth row in B_2 to the first ,we get B_3.
An Orthogonal matrix to B_3 is $M = [\ -F^T / I_4\ ] = [\ F^T / I_4]$

Thus M=

b	e	f	g	d	a	c	h	k
1	1	0	0	0	1	0	0	0
1	0	1	1	0	0	1	0	0
0	1	1	0	0	0	0	1	0
0	1	1	1	1	0	0	0	1

Before M can be regarded as a reduced incidence matrix, it must have at most two I^s in each column. This can be achieved by adding (mod 2) the third row to the fourth in M, giving M^1.

Thus M^1 =

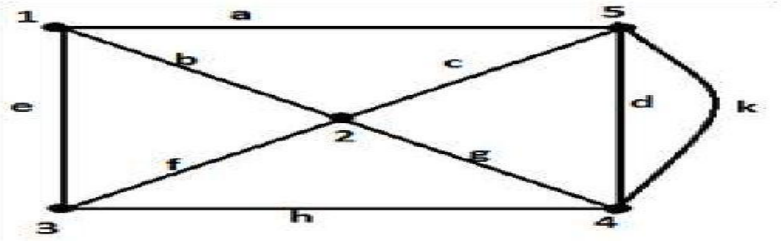
b	e	f	g	d	a	c	h	k
1	1	0	0	0	1	0	0	0
1	0	1	1	0	0	1	0	0
0	1	1	0	0	0	0	1	0
0	1	1	1	1	0	0	0	1

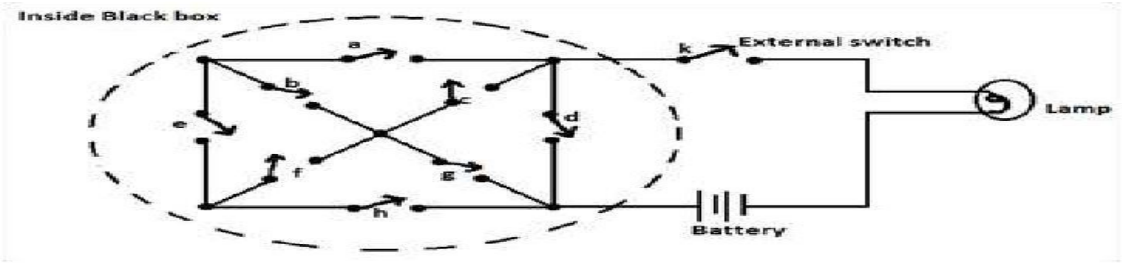
Matrix M^1 is the reduced incidence matrix .The incidence matrix A can be obtained by adding a fifth row to M^1 such that there are exactly two I^S in every column.

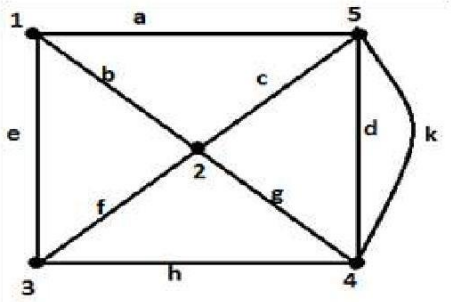
A =

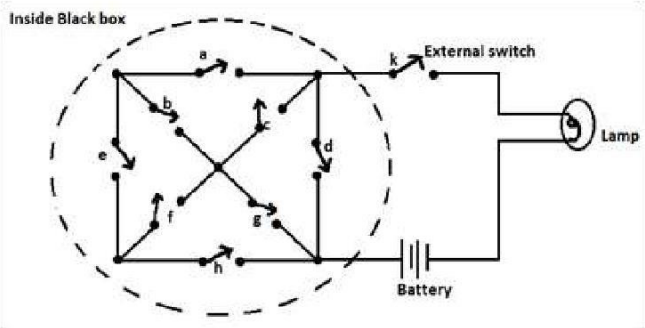
b	e	f	g	d	a	c	h	k
1	1	0	0	0	1	0	0	0
1	0	1	1	0	0	1	0	0
0	1	1	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	0	1

From the above incidence matrix A we are able to construct the graph and hence the corresponding switching network as shown below.


1
a
5
b
c
e
d
k
2
f
g
3
h
4


Inside Black box
a
k
External switch
b
c
e
d
Lamp
f
g
h
Battery


1
a
5
b
c
e
d
k
2
f
g
3
h
4


Inside Black box
a
k
External switch
b
c
e
d
Lamp
f
g
h
Battery

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CONCLUSION

Thus by removing the obviously redundant circuits and by constructing the incidence matrix, we see that the corresponding switching networks inside a box can be found without opening it.

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